Abstracts

Spiral inductors and transmission lines in silicon technology using copper-damascene interconnects and low-loss substrates

J.N. Burghartz, D.C. Edelstein, K.A. Jenkins and Y.H. Kwark. "Spiral inductors and transmission lines in silicon technology using copper-damascene interconnects and low-loss substrates." 1997 Transactions on Microwave Theory and Techniques 45.10 (Oct. 1997, Part II [T-MTT] (Special Issue on Interconnects and Packaging)): 1961-1968.

Spiral inductors and different types of transmission lines are fabricated by using copper (Cu)-damascene interconnects and high-resistivity silicon (HRS) or sapphire substrates. The fabrication process is compatible with the concepts of silicon device fabrication. Spiral inductors with 1.4-nH inductance have quality factors (Q) of 30 at 5.2 GHz and 40 at 5.8 GHz for the HRS and the sapphire substrates, respectively. 80-nH inductors have Q's as high as 13. The transmission-line losses are near 4 dB/cm at 10 GHz for microstrips, inverted microstrips, and coplanar lines, which are sufficiently small for maximum line lengths within typical silicon-chip areas. This paper shows that inductors with high Q's for lumped-element designs in the 1-10-GHz range and transmission lines with low losses for distributed-element designs beyond 10 GHz can be made available with the proposed adjustments to commercial silicon technology.

❑ Return to main document.